REMARKS

Applicants note the filing of an Information Disclosure Statement herein on June 16, 2003. Applicants respectfully request that the information cited on the PTO-1449 be made of record herein.

The Final Office Action mailed May 27, 2003, has been received and reviewed. Claims 1, 4 through 10, and 13 through 20 are currently pending in the application. New claims 21-24 are proposed. Claims 1, 4 through 10, and 13 through 20 stand rejected. Applicants propose to amend claims 1, 9 and 10. Reconsideration is respectfully requested.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,274,423 to Prall et al. Previously Applied, in View of U.S. Patent No. 6,124,626 to Sandhu et al.

Claims 1, 4, 6 through 10, 13 through 15, and 17 through 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Prall et al. (U.S. Patent No. 6,274,423) previously applied, in view of Sandhu et al. (U.S. Patent No. 6,124,626). Applicants respectfully traverse this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Prall discloses an etch process for aligning a capacitor and an adjacent contact corridor. Sandhu discloses capacitor structures formed using excess oxygen containing materials.

By way of contrast with Prall and Sandhu, claim 1 of the presently claimed invention recites a "DRAM circuit comprising: a substrate having a an active region thereon and capacitor structure disposed above said active region, said capacitor structure including a storage node, a

dielectric layer overlying said storage node, and a conductive cell plate overlying said dielectric layer, each of said dielectric layer and said conductive cell plate having an end portion proximate a conductive contact, said conductive contact extending downward and adjacently beside said capacitor structure, said end portion of said dielectric layer extending closer to said conductive contact than said end portion of said conductive cell plate; a first TEOS layer disposed proximate said storage node; a second TEOS layer disposed over said capacitor structure and encasing said end portions of said dielectric layer and said conductive cell plate, said second TEOS layer disposed between said capacitor structure and said conductive contact; and a doped BPSG layer disposed over said second TEOS layer, said conductive contact extending through said BPSG layer and said second TEOS layer."

Applicants respectfully submit that the proposed combination of references fails to teach or suggest every element of claim 1 of the presently claimed invention. The combination of Prall and Sandhu fails to teach or suggest a first TEOS layer disposed proximate said storage node and a second TEOS layer over said capacitor structure and encasing said end portions of said dielectric layer and said conductive cell plate, said second TEOS layer disposed between said capacitor structure and said conductive contact. As the proposed combination of references fails to teach or suggest every element of the presently claimed invention, applicants submit that independent claim 1 is not rendered obvious by the cited references. Thus, claim 1 is allowable.

Further, applicants respectfully submit that no motivation exists in the cited references for their combination. Prall is directed toward an etch process for aligning a capacitor structure and adjacent contact corridor. Sandhu discloses that the ozone enhanced TEOS layer protects against oxygen leaks. Sandhu lacks any disclosure that a TEOS layer would provide any benefit to the capacitor structure in Prall. Further, as Sandhu fails to teach or suggest end portions proximate a conductive contact, no motivation exists to form a TEOS layer that encases end portions of the dielectric layer and conductive cell plate in Prall. As no motivation exists to combine the references, applicants submit that independent claim 1 of the presently claimed invention is not rendered obvious. Thus, claim 1 is allowable.

Claims 4 through 9, 21 and 22 are each allowable as depending, either directly or indirectly, from allowable claim 1.

Claim 9 is further allowable as neither Prall nor Sandhu teaches or suggests that the TEOS layer is a dopant barrier between the capacitor structure and the BPSG layer.

New claim 21 is further allowable as neither Prall nor Sandhu teaches or suggests the first TEOS layer is configured to prevent diffusion of contaminants into the active region.

New claim 22 is further allowable as neither Prall nor Sandhu teaches or suggests the first TEOS layer comprises a thickness of about 100 Å to about 250 Å.

Independent claim 10 of the presently claimed invention is allowable at least for the same reasons as independent claim 1 of the presently claimed invention. By way of contrast with Prall and Sandhu, claim 10 of the presently claimed invention recites a "semiconductor memory device comprising: a semiconductor substrate having an active region thereon and a capacitor structure formed above said active region, said capacitor structure including a first conductive layer, a second conductive layer, and a dielectric layer, said dielectric layer disposed between said first and second conductive layers, each of said dielectric layer and said first and second conductive layers having an end portion proximate a conductive contact, said conductive contact extending downward and adjacently beside said capacitor structure, said end portion of said dielectric layer extending closer to said conductive contact than said end portion of each of said first conductive layer and said second conductive layer; a diffusion barrier proximate said first conducting layer and configured to prevent diffusion of contaminants into said active region; a TEOS layer disposed over said capacitor structure and encasing said end portions of said dielectric layer and each of said first conductive layer and said second conductive layer, said TEOS layer disposed between said capacitor structure and said conductive contact; and a doped BPSG layer disposed over said TEOS layer, said conductive contact extending through said BPSG layer and said TEOS layer."

Applicants respectfully submit the proposed combination of Prall and Sandhu fails to teach or suggest every element of the presently claimed invention. Specifically, neither Prall nor Sandhu teach or suggest "a diffusion barrier proximate said first conducting layer and configured to prevent diffusion of contaminants into said active region" or "a TEOS layer disposed over said capacitor structure and encasing said end portions of said dielectric layer and each of said first conductive layer and said second conductive layer, said TEOS layer disposed between said

capacitor structure and said conductive contact; and a doped BPSG layer disposed over said TEOS layer, said conductive contact extending through said BPSG layer and said TEOS layer."

Instead, neither reference teaches or suggests diffusion barrier proximate a first conducting layer and configured to prevent diffusion of contaminants into an active region. Further, Prall lacks fails to teach or suggest a TEOS layer, a BPSG layer disposed over said TEOS layer or a conductive contact extending through a doped BPSG layer and TEOS layer. Sandhu lacks disclosure of end portions of dielectric layer, first conductive layer and second conductive layer or any conductive contact. As the proposed combination of references fails to teach or suggest every element of the presently claimed invention, applicants submit that independent claim 10 is not rendered obvious by the cited references. Thus, claim 10 is allowable.

Further, applicants respectfully submit that no motivation exists in the cited references for their combination. Prall is directed toward an etch process for aligning a capacitor structure and adjacent contact corridor. Sandhu discloses that the ozone enhanced TEOS layer protects against oxygen leaks. Sandhu lacks any disclosure that a TEOS layer would provide any benefit to the capacitor structure in Prall. Further, as Sandhu fails to teach or suggest end portions proximate a conductive contact, no motivation exists to form a TEOS layer that encases end portions of the dielectric layer and conductive cell plate in Prall. As no motivation exists to combine the references, applicants submit that independent claim 10 of the presently claimed invention is not rendered obvious. Thus, claim 10 is allowable.

Claims 13 through 20 are each allowable as depending, either directly or indirectly, from allowable claim 10.

Claim 20 is further allowable as neither Prall nor Sandhu teaches or suggests that the TEOS layer is a dopant barrier between the capacitor structure and the BPSG layer.

New claim 23 is further allowable as neither Prall nor Sandhu teaches or suggests a diffusion barrier comprising a nitride layer or TEOS layer.

New claim 24 is further allowable as neither Prall nor Sandhu teaches or suggests a diffusion barrier comprising a thickness of about 100 Å to about 250 Å.

Obviousness Rejection Based on U.S. Patent No. 6,274,423 to Prall et al. Previously Applied, and U.S. Patent No. 6,124,626 to Sandhu et al. Previously Applied, as Applied to Claims 1-4, 6-9, 10-15 and 17-20 Above, and Further in View of U.S. Patent No. 5,763,306 to Tsai Previously Applied

Claims 5 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Prall et al. (U.S. Patent No. 6,274,423) previously applied, and Sandhu et al. (U.S. Patent No. 6,124,626) previously applied, as applied to claims 1-4, 6-9, 10-15 and 17-20 above, and further in view of Tsai (U.S. Patent No. 5,763,306) previously applied. Applicants respectfully traverse this rejection, as hereinafter set forth.

The Court of Appeals for the Federal Circuit has stated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also MPEP § 2143.03. Having failed to teach or suggest each and every limitation of the current application, the prior art referenced as rendering dependent claims 5 and 16 obvious, cannot serve as a basis for rejection.

ENTRY OF AMENDMENTS

The proposed amendments to claims 1, 9 and 10 and new claims 21 through 24 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. For example, the proposed claim amendments are supported by the as-filed specification, at least paragraphs [0020] and [0024].

Further, the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1, 4 through 10 and 13 through 24 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,

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